AMENDMENTS TO THE CLAIMS

Please amend claims 1, 3-8, 16 and 18-20 in accordance with the following list of claims:

1. (Currently Amended) A semiconductor chip package comprising:

a first integrated semiconductor chip having a one side and a reverse side, and having a first electrode for wiring on the ~~first chip~~ one side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface;

a second integrated semiconductor chip having a one side and a reverse side, and having a second electrode for wiring on the ~~second chip on~~ one side of the second integrated semiconductor chip, the second integrated semiconductor chip being mounted on the ~~interposer substrate~~ first surface of the interposer substrate with the ~~second chip~~ one side of the second integrated semiconductor chip facing the ~~interposer substrate~~ first surface of the interposer substrate, such that the second electrode is exposed through the through-hole, the second electrode to be wired through the through-hole to external terminals on the ~~interposer substrate~~ second surface of the interposer substrate,

the first integrated semiconductor chip being mounted on the ~~second chip~~ reverse side of the second integrated semiconductor chip with the ~~first chip~~ reverse side of the first integrated semiconductor chip facing the ~~second chip~~ reverse side of the second integrated semiconductor chip.

2. (Canceled)

3. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the ~~first chip~~ one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size, having a one side and a reverse side, and having a second electrode for wiring on the ~~second chip~~ one side of

the second integrated semiconductor chip, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the ~~second chip~~ reverse side of the second integrated semiconductor chip facing the ~~first chip~~ reverse side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface, the through-hole being larger than the second chip size;

an adhesive sheet having opposite first and second surfaces, the adhesive sheet being formed of a sheet-shaped adhesive material provided on the interposer substrate at the ~~interposer substrate~~ first surface of the interposer substrate so as to cover the through-hole, the ~~adhesive sheet~~ second surface of the adhesive sheet being exposed through the through-hole from a side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate,

wherein the ~~second chip~~ reverse side of the second integrated semiconductor chip is fixed to the ~~adhesive sheet~~ second surface of the adhesive sheet, and the ~~first chip~~ reverse side of the first integrated semiconductor chip is fixed to the ~~adhesive sheet~~ first surface of the adhesive sheet so as to face the ~~second chip~~ reverse side of the second integrated semiconductor chip at a position at which the second integrated semiconductor chip is fixed, whereby the second electrode can be wired to external terminals on the ~~interposer substrate~~ second surface of the interposer substrate.

4. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the ~~first chip~~ one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size and having a one side and a reverse side, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the ~~second chip~~ reverse side of the second integrated semiconductor chip facing the ~~first chip~~ reverse side of the first integrated semiconductor chip; and

an interposer substrate having a through-hole, the through-hole being smaller than the first chip size and larger than the second chip size,

wherein the first integrated semiconductor chip is mounted via an adhesive sheet on the ~~interposer substrate~~ first surface of the interposer substrate at a portion of the ~~first chip~~ reverse side of the first integrated semiconductor chip, such that the through-hole is covered by the first integrated semiconductor chip and the adhesive sheet, and

wherein the ~~second chip~~ reverse side of the second integrated semiconductor chip is fixed to the ~~first chip~~ reverse side of the first integrated semiconductor chip, the adhesive sheet on the ~~first chip~~ reverse side of the first integrated semiconductor chip being exposed through the through-hole from a side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate.

5. (Currently Amended) A semiconductor chip package according to claim 1, wherein the interposer substrate has a sunken region, which is sunken into the side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate, and the through-hole is provided through the sunken region.

6. (Currently Amended) A semiconductor chip package according to claim 3, wherein the interposer substrate has, a sunken region, which is sunken into the side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate, and the through-hole is provided through the sunken region.

7. (Currently Amended) A semiconductor chip package according to claim 4, wherein the interposer substrate has a sunken region, that is sunken into the side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate, and the through-hole is provided through the sunken region.

8. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the ~~first chip~~ one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size, having a one side and a reverse side, and having a second electrode for wiring on the ~~second chip~~ one side of the second integrated semiconductor chip, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the ~~second chip~~ reverse side of the second integrated semiconductor chip facing the ~~first chip~~ reverse side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface; and

an adhesive sheet formed of sheet-shaped adhesive material at the ~~interposer substrate~~ first surface of the interposer substrate so as to cover the through-hole, the adhesive sheet being larger than the second chip size and having a hole smaller than the second chip size,

wherein the second integrated semiconductor chip is fixed, at the ~~second chip~~ one side of the second integrated semiconductor chip, to the ~~interposer substrate~~ first surface of the interposer substrate via the adhesive sheet, and

wherein the second electrode for wiring is exposed from the side of the interposer substrate at the ~~interposer substrate~~ second surface of the interposer substrate through the adhesive sheet small hole and the ~~interposer substrate~~ through-hole of the interposer substrate.

9. (Previously Presented) A semiconductor chip package according to claim 1, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

10. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

11. (Previously Presented) A semiconductor chip package according to claim 4, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

12. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate is formed of one of a nonconductive tape and a glass epoxy material.

13. (Previously Presented) A semiconductor chip package according to claim 3, wherein both surfaces of the adhesive sheet become viscous when heated.

14. (Previously Presented) A semiconductor chip package according to claim 8, wherein both surfaces of the adhesive sheet become viscous when heated.

15. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate has external terminals on its second surface to which the second electrode can be wired, and external terminals on its first surface to which the first electrode can be wired.

16. (Currently Amended) A semiconductor chip package according to claim 15, further comprising:

a plurality of solder balls mounted to the ~~interposer substrate~~ second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

17. (Previously Presented) A semiconductor chip package according to claim 4, wherein the interposer substrate has external terminals on its second surface to which the second electrode can be wired, and external terminals on its first surface to which the first electrode can be wired.

18. (Currently Amended) A semiconductor chip package according to claim 17, further comprising:

a plurality of solder balls mounted to the ~~interposer substrate~~ second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

19. (Currently Amended) A semiconductor chip package according to claim 3, wherein the interposer substrate has external terminals on its first surface to which the first electrode can be wired, and the semiconductor chip package further comprises a plurality of solder balls mounted to the ~~interposer substrate~~ second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

20. (Currently Amended) A semiconductor chip package according to claim 1, wherein the interposer substrate has external terminals on its first surface to which the first electrode can be wired, and the semiconductor chip package further comprises a plurality of solder balls mounted to the ~~interposer substrate~~ second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.